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**EXPERIMENT NO: 6**

**Design of Logic gates using Complementary MOSFET (CMOS)**

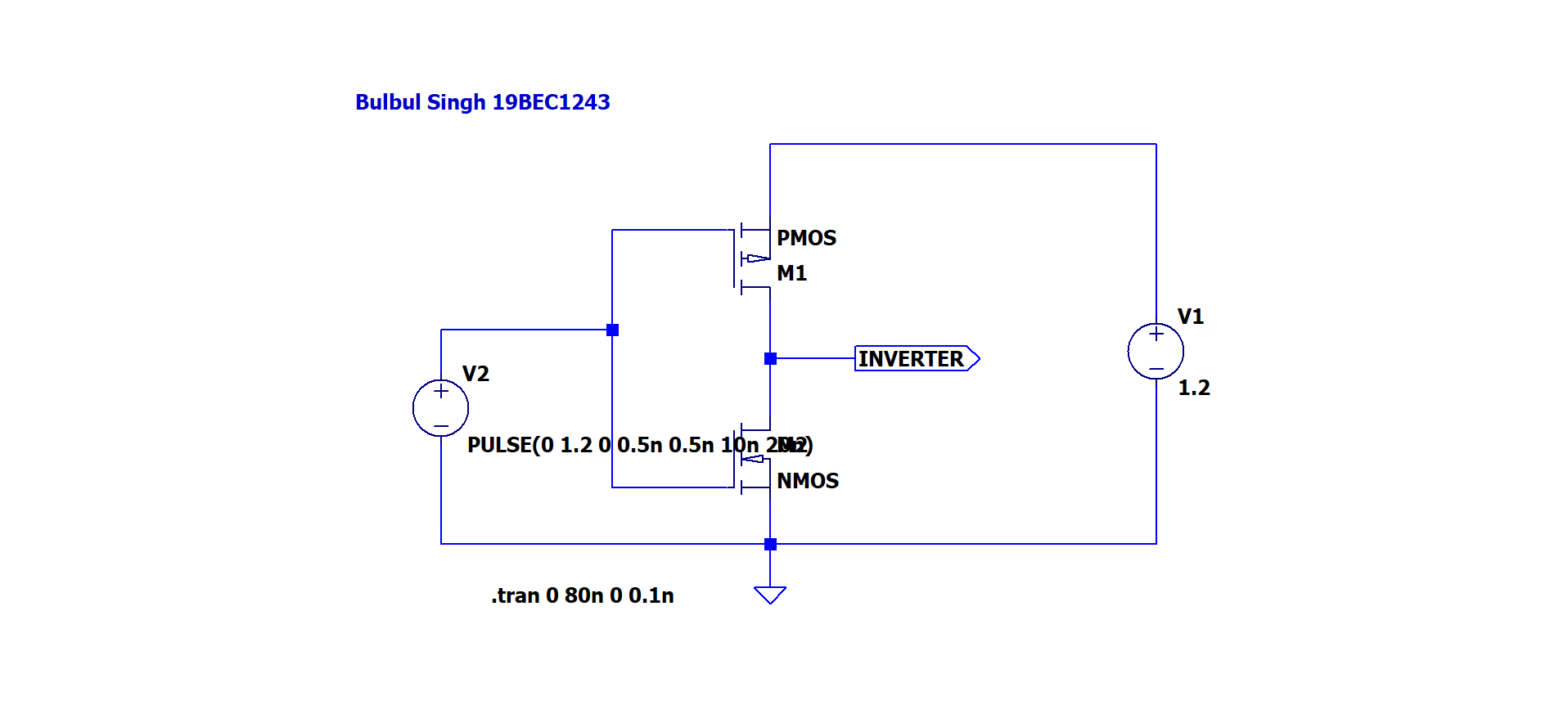
**Aim:** To design Logic gates using Complementary MOSFET (CMOS) in LTSpice.

**Software used:** LTSpice

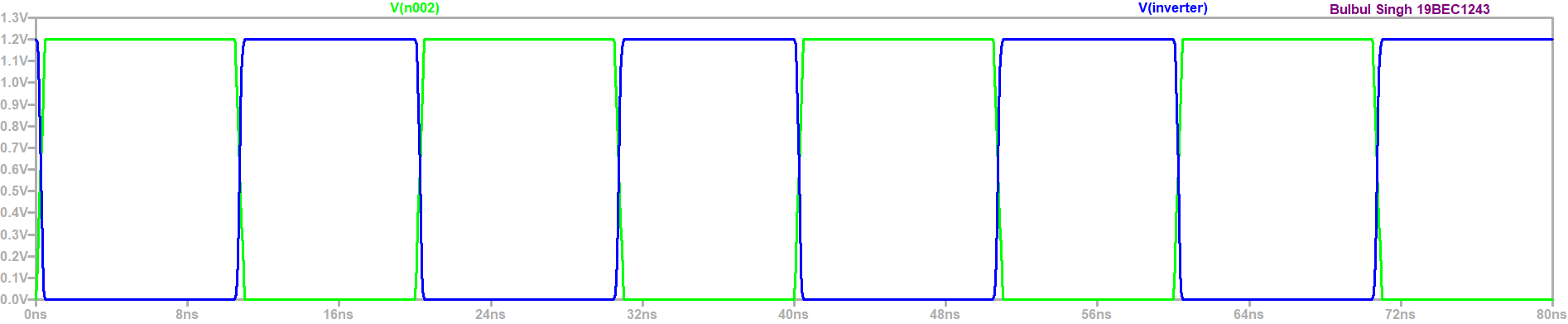
**Components required:** Voltage source, cmosn, cmosp.

**Task 1: Implementation of Inverter**

**Circuit:**

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**Output:**

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**Truth Table:**

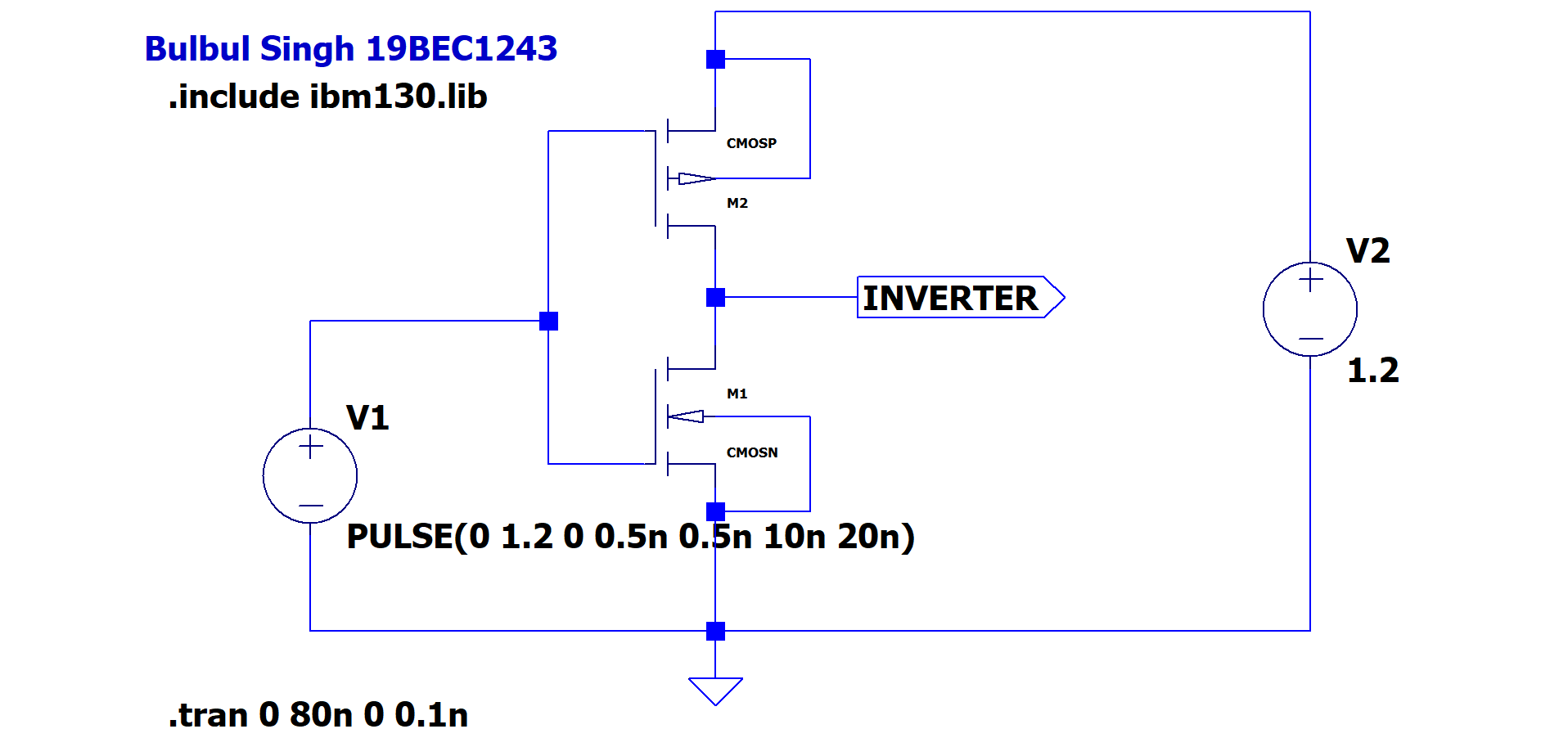
|  |  |
| --- | --- |
| **Vin** | **Vout** |
| 1 | 0 |
| 0 | 1 |

**Conclusion:**

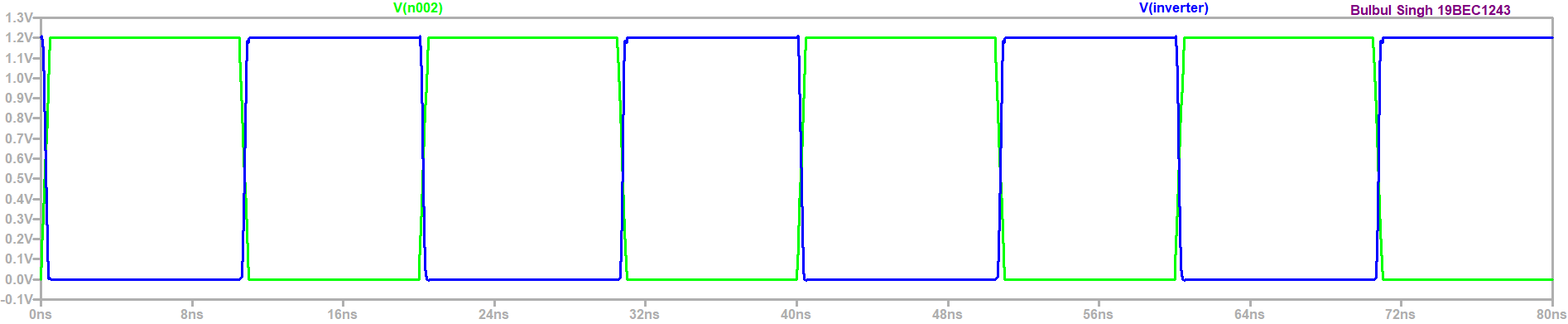
From above graph we can observe that output is high when input is low and low when input is high. Thus, an inverter is implemented using PMOS and NMOS.

**Task 2: Implementation of Inverter using CMOS**

**Circuit:**

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**Output:**

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**Truth Table:**

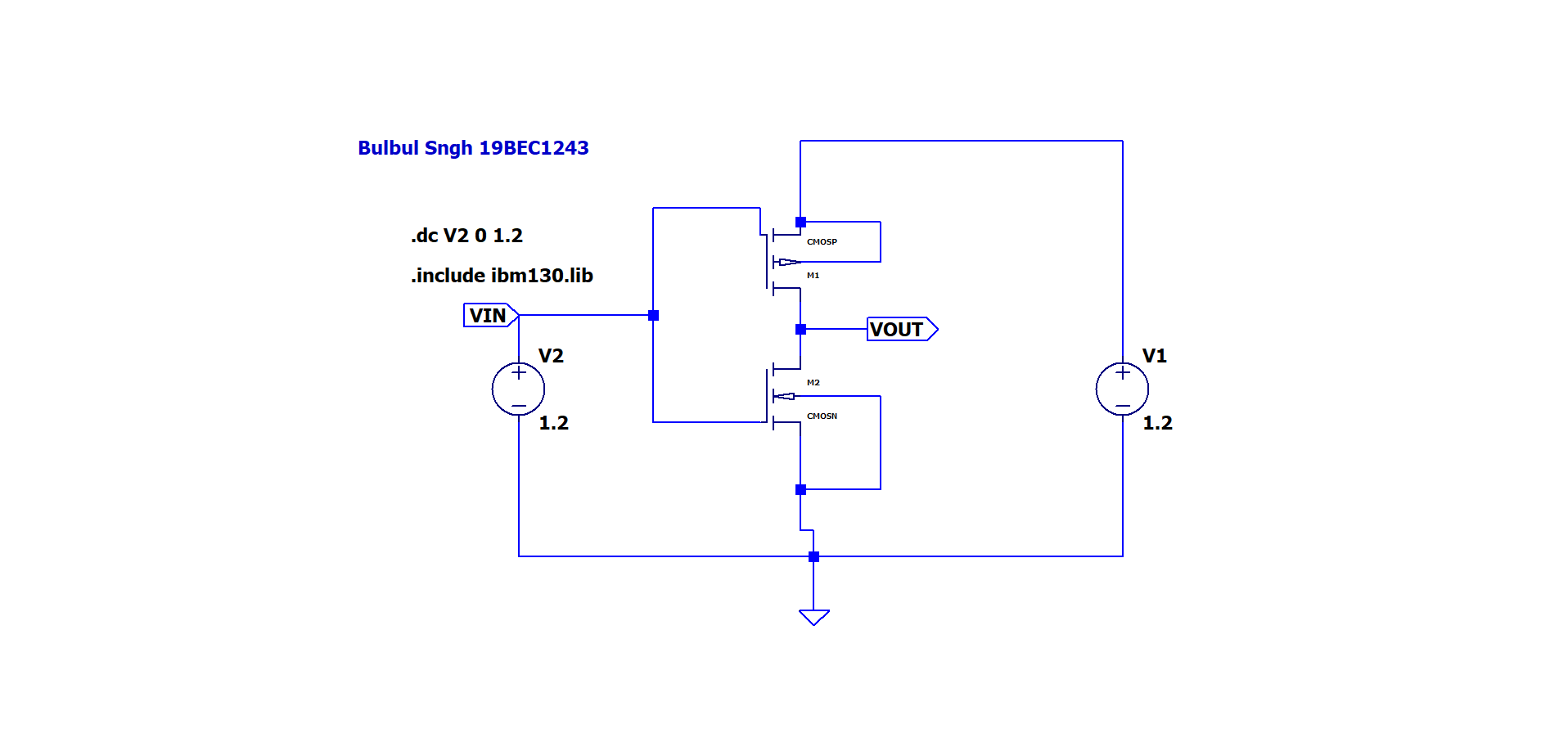
|  |  |
| --- | --- |
| **Vin** | **Vout** |
| 1 | 0 |
| 0 | 1 |

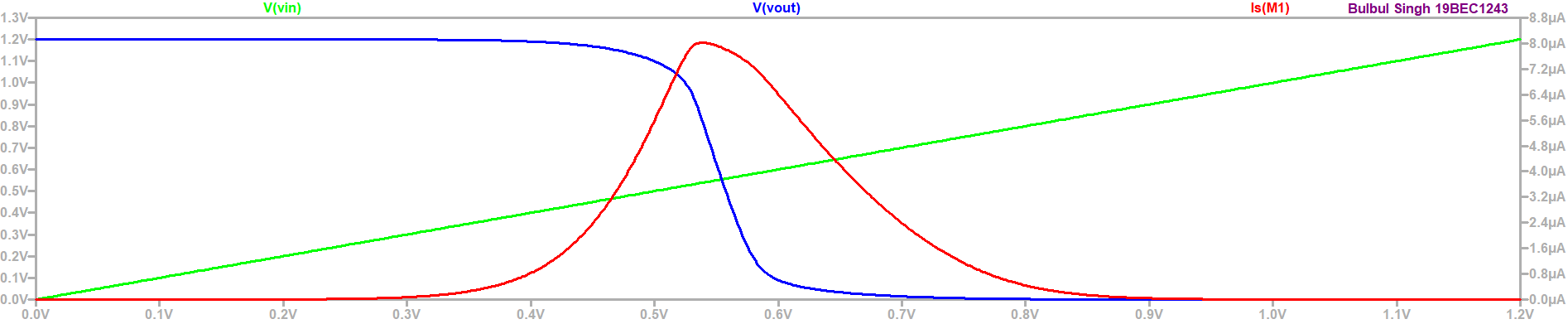
**Conclusion:**

From above graph we can observe that output is high when input is low and low when input is high. Thus, an inverter is implemented using CMOSN AND CMOSP.

**Task 3:** **To study transition characteristics of Inverter using 130nm technology**

**Circuit:**

**Output:**

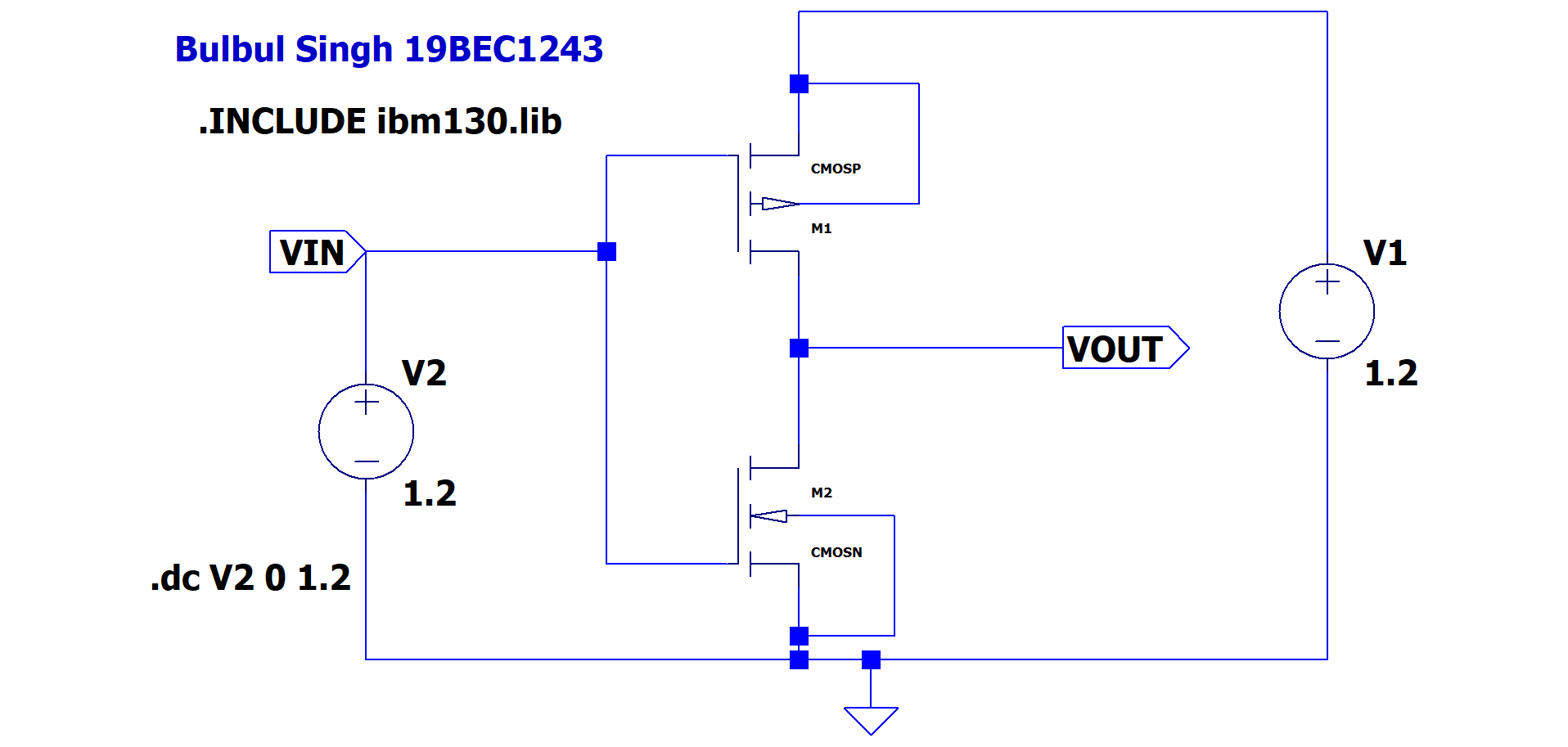
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**Conclusion:**

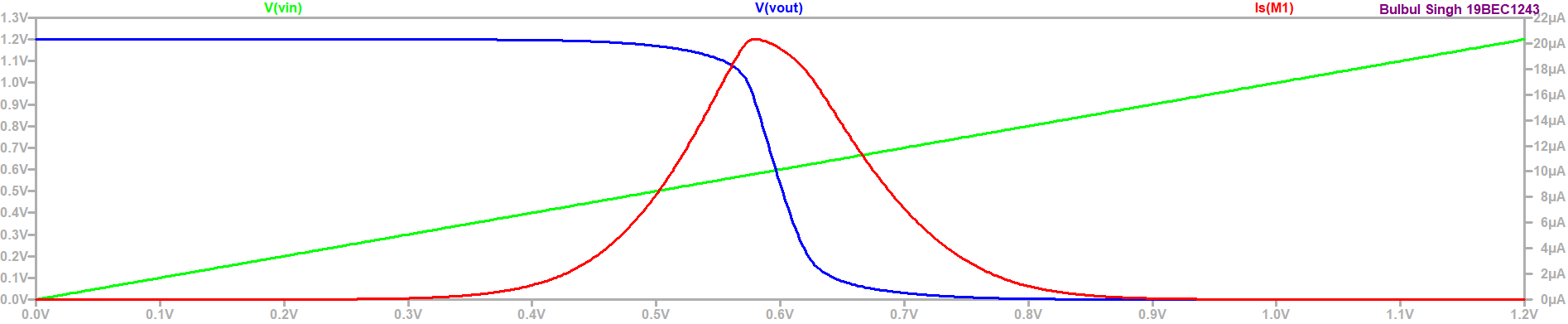
From above graph we can observe that transition region is from 0.3 V to 0.9 V and also, Vin and Vout do not intercept at 0.6V point.

**Task 4: To study transition characteristics of Inverter using 130nm technology: Symmetric**

**Circuit :**

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**Output:**

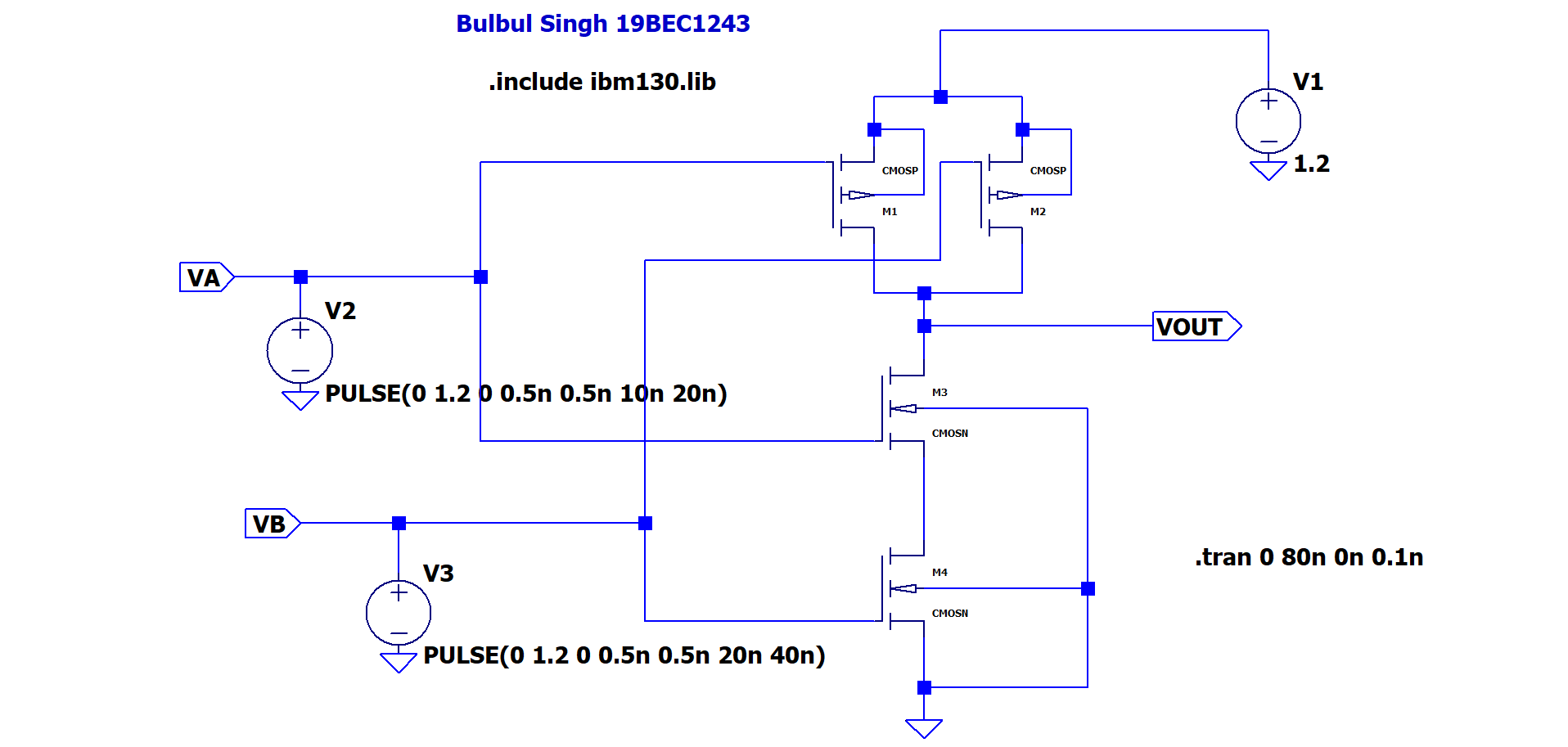
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**Conclusion:**

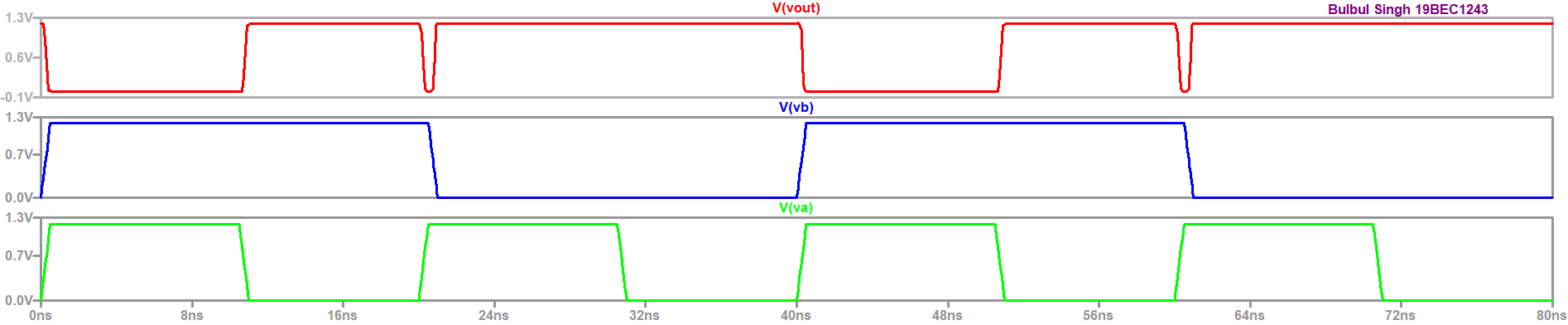
From above graph we can observe that transition region is from 0.3V to 0.9 V and Vin and Vout intercept at 0.6V point because of Symmetric properties.

**Task 5: To implement NAND gate using CMOS**

**Circuit:**

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**Output:**

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**Truth Table:**

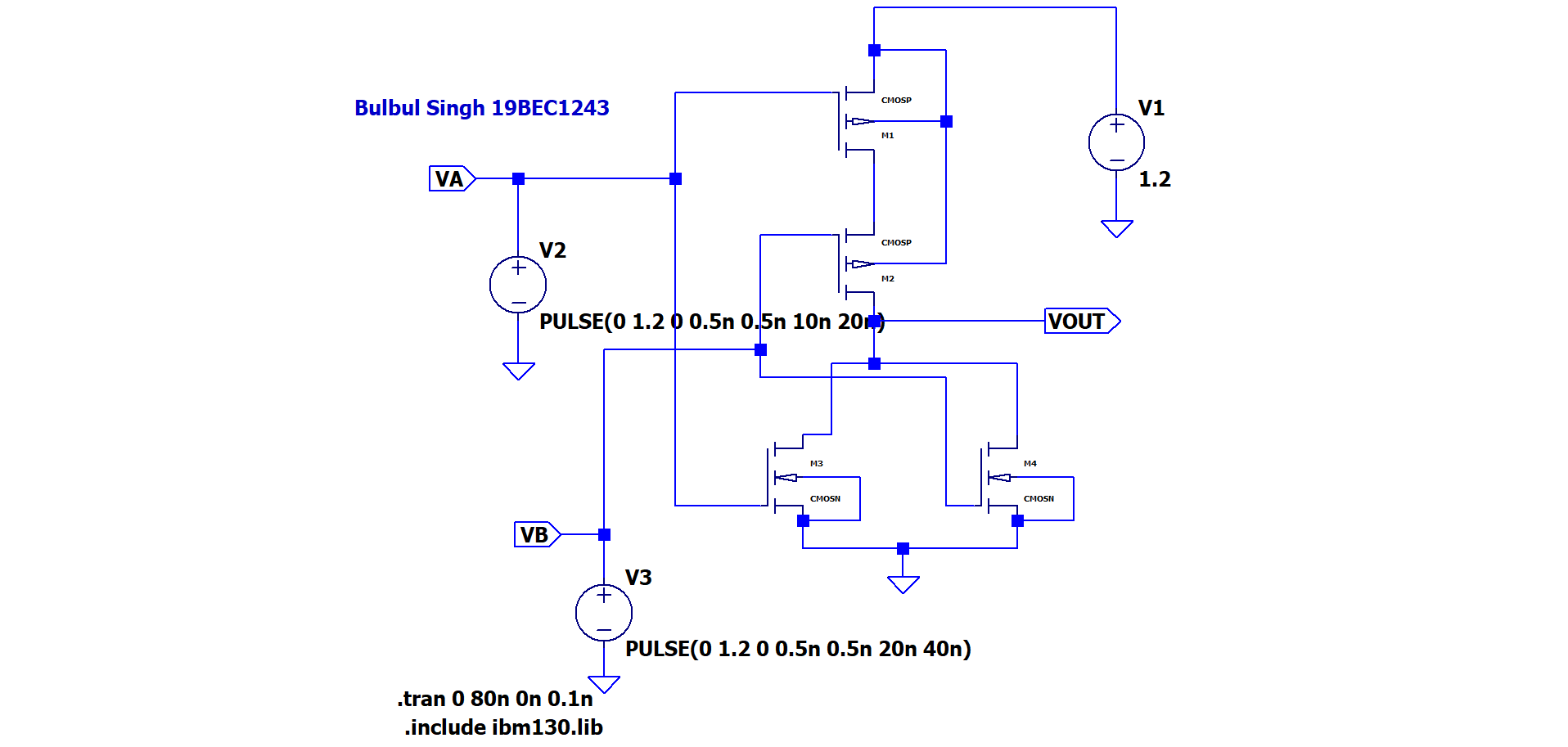
|  |  |  |
| --- | --- | --- |
| **V\_A** | **V\_B** | **V\_out** |
| 0 | 0 | 1 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

**Conclusion:**

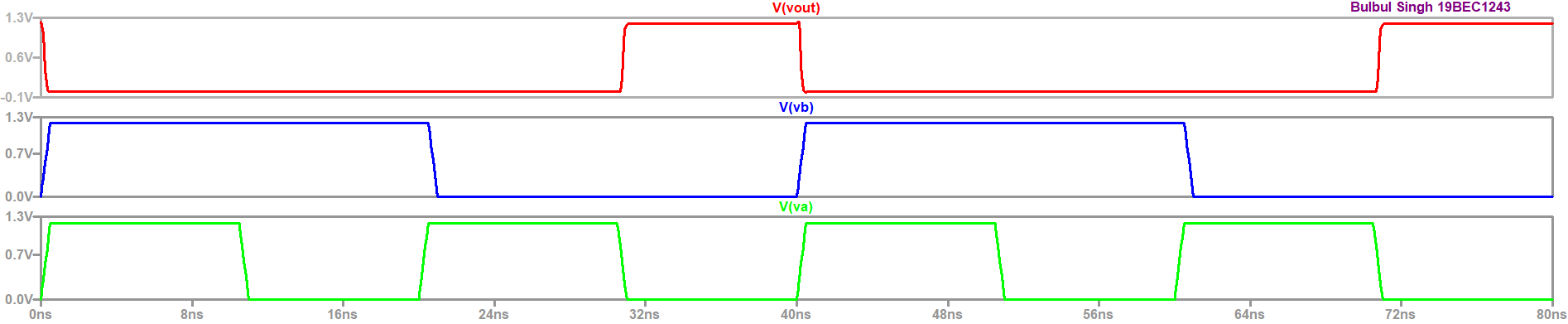
From the above graph we can observe that when both inputs are high, output is low while in all other cases it is high thus, it satisfies the truth table.

**Task 6**: To implement NOR gate using CMOS

**Circuit:**

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**Output:**

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**Truth Table:**

|  |  |  |
| --- | --- | --- |
| **V\_A** | **V\_B** | **V\_out** |
| 0 | 0 | 1 |
| 0 | 1 | 0 |
| 1 | 0 | 0 |
| 1 | 1 | 0 |

**Conclusion:**

From the above graph we can observe that when both inputs are low, output is high while in all other cases it is low thus, it satisfies the truth table.